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EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	**PAPER NUMBER**
2183	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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1. Continuation of Box 13

2. **Applicant's Arguments**:

Applicant's argued 35 USC 112 1st rejection and indicating that the specification supports the new matter limitation "*without computing a memory address equaling the first base address value added to the offset address value in detecting the first instruction".* Furthermore, the applicant's refer to pages 4 and 6 of the specifications:

> The invention provides a method and system for operating a pipelined microprocessor more quickly, by detecting instructions without having to actually compute the referenced external memory address. (See Specification page 4, lines 3-6)
>
> The instruction decode stage 120 parses the instructions 151 to determine what types of instructions 151 they are (such as instructions 151 that load data from external memory or store data to external memory). As part of parsing the instructions 151, and in **addition to determine what operations** the instructions 151 command the microprocessor to perform, the instruction decode stage 120 determines the syntax of any address in external memory that the instructions 151 refer to as operands. (See Specification page 6, lines 17-22) (Emphasis added)

Examiner's Response:

The examiner respectfully disagrees because applicant's specification does not explain or show the current claim language (new matter limitation) "*without computing a memory address equaling the first base address value added to the offset address value in detecting the first instruction".* The specification does not show a memory address equaling **the first base address value added to the offset address value** is <u>not computed</u> in detected the first

instruction. The specification shows that the referenced external memory address is not computed (specification page 4, lines 3-6) but there is not mentioning of "first base address value **added** to the offset address value". Therefore the argued limitation stand as previously rejected.

Furthermore, as explained in the previous final action, obviousness is not the test for written description and it is not a question of whether one skilled in the art might be able to construct the patentee's device from the teachings of the disclosure…Rather, it is a question of whether the disclosure necessarily discloses that particular device.

3. Applicant's Arguments:

"Applicant's argues that the feature "*detecting a first instruction using first base and offset address values to load data from a first memory location that was previously stored to, wherein the first instruction is detected based upon the first base and offset address values and without using a memory address equaling to the first base address value added to the offset address value*" is not found in the cited references. *Yeager* teaches comparing virtual addresses that are, for indexed address calculations, formed by "base+index." *Yeager* column 9, lines 21-22. *Hesson et al* does not, as asserted in the Office Action, teach that the virtual addresses employed have **base and effective addresses**"

Examiner's Response:

The examiner respectfully disagrees with appellant's argument for a number of reasons. First, the examiner would like to remind the applicant's that the rejection is based on the broadest reasonable interpretation of the claim language along with explicit and unambiguous definition for the claim language which must be made available in the specification. The instant specification

clearly fails to show or explain the feature of the claim language "*without computing a memory address equaling the first base address value added to the offset address value in detecting the first instruction".* Therefore, this limitation is given its broadest reasonable interpretation.

With regards to Yeager references, the examiner respectfully disagrees because Yeager (abstract) clearly indicates that "*dependencies are tracked **before virtual addresses are actually calculated**".* Therefore, the dependencies of memory access instructions are detected **before computing a memory address** which reads on claimed language "***without computing a memory address**...*"

With regards to Hesson, **the bits of the virtual address** that are used for comparison are considered to be equivalent to **the base and offset address**. However, the bits of the virtual address of Hesson are not computed by adding two addresses (base plus offset).

4. **Applicant's Arguments**:

"Claim 20 recites using the syntax for the first instruction and the syntax for the second instruction to determine a relationship between the first memory location and the second memory location, without using the effective address for the first memory location or the effective address for the second memory location. Such a feature is not found in the cited references. Both *Yeager* and *Hesson et al* teach using the virtual addresses - that is, the effective addresses, as opposed to the physical or "real" addresses - of memory locations to determine correspondence of two memory locations. The interpretation of "using the effective address for the first memory location" as being limited to "using the effective address to access the memory location is arbitrary and capricious. No basis for such as limitation, other than to contrive a basis for rejection of the claim, exists."

Examiner's response:

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., physical or real addresses) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, virtual addresses are equivalent to the claimed memory addresses. Also, as indicated by both references, virtual addresses are mapped to physical address (see for instance, Yeager, col. 5, lines 20-23).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

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